REMARKS

This application has been carefully reviewed in light of the Office Action dated March 10, 2004. Claims 1-20 remain in this application. Claims 1, 10, 13, 15, 17 and 18 are the independent Claims. It is believed that no new matter is involved in the arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Priority

On page 2 of the Office Action, the Examiner requests a certified copy of the Japanese application corresponding to the present application. In response, Applicant states that there is no foreign counterpart to the present application

Objection to the Abstract

The Abstract Of The Disclosure was objected to for exceeding 150 words. In response, Applicant has amended the abstract to address the Examiner's objection. Reconsideration and withdrawal of the above objection are respectfully requested.

Request for Serial No. of related application

On page 3 of the Office Action requests the application Serial No. disclosed in the specification before the first line. Applicant responds that the requested Serial No. is 10/092/356.

Double Patenting Rejections

Claims 1-20 were rejected under the judicially created doctrine of obviousness-type double patenting over Claims 1-10 of U.S. Patent No. 6,366,065 ("Morita") in view of U.S. Patent No. 6,160,533 (Tamai). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the arguments presented

below.

The Morita Reference

The Morita reference discloses a voltage supplying device which supplies a voltage to a load capacitance to finish charging the load capacitance with a predetermined voltage within a predetermined charging period. (*See, Morita, abstract; Col. 1, lines 6-9*). According to the applied Claim 1 of Morita a first switching element is provided between the impedance conversion circuit and the load capacitance. A bypass line is provided for bypassing the impedance conversion circuit and the first switching element and supplying from the voltage supplying source to the load capacitance. A second switching element is provided on the bypass line. In the first period of the charging period, the first switching element is turned on and the second switching element is turned off. In the second period of the charging period, the first switching element is turned off and the second switching element is turned on. (*See, Morita, Col. 11, line 60 to Col. 12, line 15*)

The Tamai Reference

Tamai is directed to a method and apparatus for driving a display panel such as an active matrix type liquid crystal display panel. (*See, Tamai, abstract; Col. 1, lines 6-8*). The aim of the Tamai reference is to reduce the number of connection terminals as well as the number of the analog switches ASW0 to ASW7 which are included in the source driver 12 to thereby reduce the chip size of the source driver 12 which is formed by a semiconductor integrated circuit and to reduce a cost. (*See, Tamai, Col. 2, lines 4-12; Figures 17 and 18*). Tamai seeks to accomplish this objective by providing a method and apparatus for driving a display panel in which higher level gradation is realized while the number of connection terminals and analog switches is reduced. (*See, Tamai, Col. 4, lines 43-49; Col. 8, lines 10-16*).

The Sandard for Obviousness-Type Double Patenting Rejection

According to MPEP §8.32, a double patenting rejection of the obviousness-type is "analogous to [a failure to meet] the nonobviousness requirement of 35 U.S.C. 103" except that the patent principally underlying the double patenting rejection is not considered prior art. In re Braithwaite, 379 F.2d 594, 154 USPQ 29 (CCPA 1967). ***Therefore, any analysis employed in an obviousness-type double patenting rejection parallels the guidelines for analysis of a 35 U.S.C. 103 obviousness determination.*** See, MPEP §8.32 (citing In re Braat, 937 F.2d 589, 19 USPQ2d 1289 (Fed. Cir. 1991); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985)).

The Claims are Patentable Over the Cited Reference

The present application is generally directed to a voltage supplying device that can promptly and precisely provide a required charging voltage without an offset canceling circuit.

As defined by amended independent Claim 1, a voltage supplying device includes a reference voltage generating circuit having a ladder resistance circuit to which a plurality of resisters are connected in series, which outputs a plurality of voltages divided in the ladder resistance circuit as a plurality of gamma-corrected reference voltages. A plurality of first impedance conversion circuits perforns impedance conversion on the plurality of reference voltages from the reference voltage generating circuit and outputs the converted voltages. A voltage selection circuit having a plurality of analogue switches one of which is turned on based on grayscale data is provided which selects one of the plurality of reference voltages from the plurality of first impedance conversion circuits. A second impedance conversion circuit perforns impedance conversion on a voltage from the voltage selection circuit and outputs the converted voltage. A first switching element for blocking an output of the second impedance conversion circuit is provided. A first bypass line for shorting input and output lines of the second impedance conversion circuit is also provided. A second

switching element is provided on the first bypass line. A plurality of third switching elements is provided for blocking an output of the plurality of first impedance conversion circuits. A plurality of second bypass lines for shorting input and output lines of the respective plurality of first impedance conversion circuits is provided. A plurality of fourth switching elements is provided on the respective plurality of second bypass lines. The first switching element is turned on and the second switching element is turned off in a first period of a charging period, and the first switching element is turned off and the second switching element is turned on in a second period of the charging period which follows after the first period. The plurality of third switching elements are turned off and the plurality of fourth switching elements are turned on at least in a final stage of the second period, and the plurality of third switching elements are turned on and the plurality of fourth switching elements are turned off in the other periods of the charging period.

The applied Morita reference does not disclose or suggest the above features of the claims of the present invention as defined by independent Claim 1. In particular, the cited references do not disclose or suggest "a reference voltage generating circuit having a ladder resistance circuit to which a plurality of resisters are connected in series, which outputs a plurality of voltages divided in the ladder resistance circuit as a plurality of gamma-corrected reference voltages," as required by independent Claim 1.

Moreover, Morita is not seen to disclose or suggest "a voltage selection circuit having a plurality of analogue switches one of which is turned on based on grayscale data, which selects one of the plurality of reference voltages from the plurality of first impedance conversion circuits," as required by independent Claim 1.

Furthermore, Morita does not teach or suggest "a second impedance conversion circuit which performs impedance conversion on a voltage from the voltage selection circuit and outputs the converted voltage," as required by independent Claim 1.

Furthermore, Morita is not seen to disclose or suggest "a plurality of second bypass lines for shorting input and output lines of the respective plurality of first impedance conversion circuits.

Similarly, Morita does not teach or suggest "a plurality of fourth switching elements provided on the respective plurality of second bypass lines."

The Office Action concedes that the applied Morita reference fails to teach or suggest the above features of the present invention, but nonetheless observes that these features are disclosed by the applied Tamai reference and that the combination of Morita and Tamai as to these features "would have been obvious" to one of ordinary skill in the art. Applicants respectfully traverse this position.

Under MPEP §2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Moreover, "the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." Id. (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

As MPEP §2143.01 makes clear, "***the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.***" Id. (citing In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)).

Applicant respectfully submits that the finding of obviousness in this case is based on nothing more than the invention of the present application, and is thus improper.

Tamai is directed to a method and apparatus for driving a display panel such as an active matrix type liquid crystal display panel. (*See, Tamai, abstract; Col. 1, lines 6-8*). The aim of the Tamai reference to reduce the number of connection terminals as well as the number of the analog switches ASW0 to ASW7 which are included in the source driver 12, for instance, to thereby reduce the chip size of the source driver 12 which is formed by a semiconductor integrated circuit and to reduce a cost. (*See, Tamai, Col. 2, lines 4-12; Figures 17 and 18*). Tamai seeks to accomplish this objective by providing a method and apparatus for driving a display panel in which higher level gradation is realized while the number of connection terminals and analog switches is reduced. (*See, Tamai, Col. 4, lines 43-49; Col. 8, lines 10-16*).

According to the Office Action "it would have been obvious to one of ordinary skill in the art at the [time] the invention was made to have used a reference voltage generating circuit, a voltage selection circuit, plurality of third switches and a plurality of fourth switches as taught by Tamai to the voltage supply device of U.S. Patent No. 6,366,065 so as to reduce the number of terminals for receiving the reference voltages." (See, Office Action, page 6). However, as noted above, the goal of Tamai is to reduce the number of connection terminals ***as well as*** the number of the analog switches. Accordingly, Tamai cannot be fairly cited for ***adding*** plurality of third switches and ***adding*** plurality of fourth switches to the invention of Morati. Accordingly, Applicant respectfully submits that the standard for obviousness type double patenting has not been met. Should the examiner persist in maintaining this ground of rejection, Applicants respectfully request that the Examiner provide the Applicants with an affidavit for the purpose of appeal.

Accordingly, amended independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that independent Claims 10, 13, 15 and 17-18 are similarly patentable for at least the same reasons as those cited in connection with independent Claim 1.

The remaining claims depend either directly or indirectly from independent Claims 1, 10, 13, 1 and 17-18 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

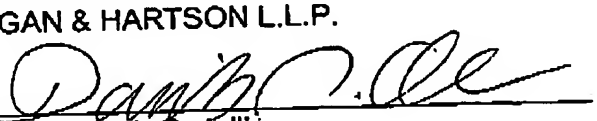
Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

By: 
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